DATA SHEET

SA56614-XX

CMOS system reset

Product data

Supersedes data of 2003 Jul 31

2003 Oct 30

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# CMOS system reset   SA56614-XX

GENERAL DESCRIPTION

The SA56614-XX is a CMOS device designed to generate a reset signal for a variety of microprocessor and logic systems. Accurate reset signals are generated during momentary power interruptions, or whenever power supply voltages sag to intolerable levels. Several reset threshold versions of the device are available. A totem-pole output topology is incorporated to provide both current source and sink capability to the user.

SA56614-XX is available in a 5-lead small outline package (SOP003).
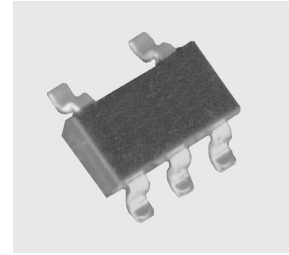
FEATURES

- 10 V_{DC} maximum operating voltage
- Low operating voltage (0.95 V)
- Totem pole CMOS output
- Offered in reset thresholds of
  1.85, 2.0, 2.7, 2.8, 2.9, 3.0, 3.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7 V_{DC}
- Available in 5-lead small outline surface mount package

APPLICATIONS

- Microcomputer systems
- Logic systems
- Battery monitoring systems
- Back-up power supply circuits
- Voltage detection circuits
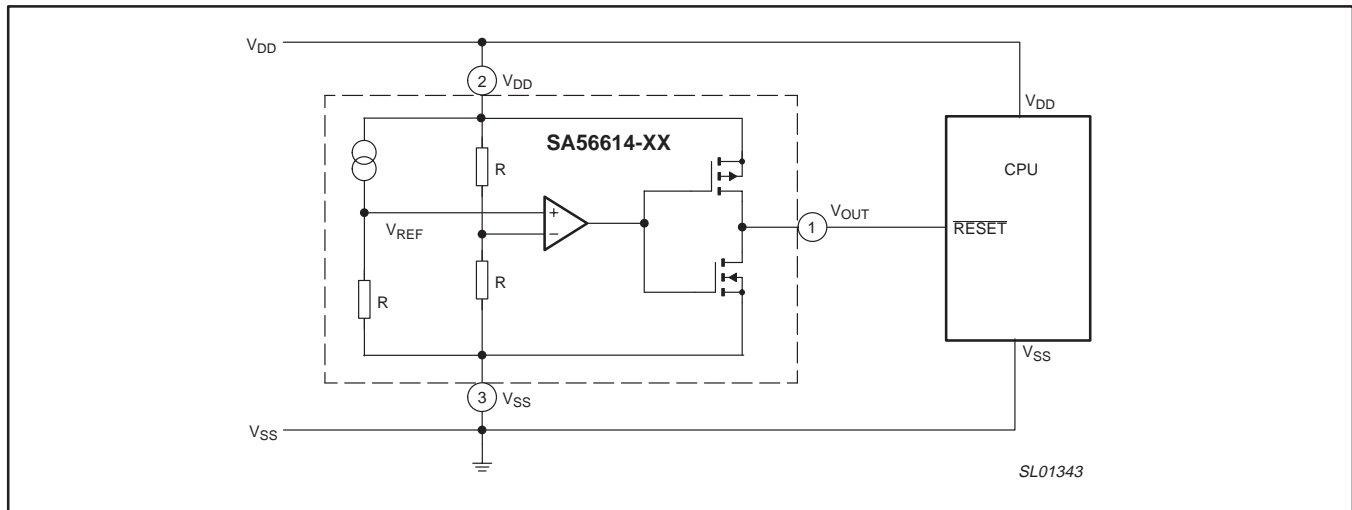
SIMPLIFIED SYSTEM DIAGRAM

Figure 1. Simplified system diagram.

CMOS system reset

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ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | | TEMPERATURE RANGE |
	NAME	DESCRIPTION	VERSION	
SA56614-**XX**GW	SOT23-5, SOT25, SO5	Plastic small outline package; 5 leads; body width 1.6 mm	SOP003	–40 to +85 °C

NOTE:
The device has thirteen detection voltage options, indicated by the XX on the 'Type number'.

XX	DETECT VOLTAGE (Typical)
185	1.85 V
20	2.0 V
27	2.7 V
28	2.8 V
29	2.9 V
30	3.0 V
31	3.1 V
42	4.2 V
43	4.3 V
44	4.4 V
45	4.5 V
46	4.6 V
47	4.7 V

Marking code
Each device is marked with a four letter code. The first three letters designate the product. The fourth, represented by an 'x', designates the date tracking code.

Part	Marking
SA56614-185GW	ABWx
SA56614-20GW	AAUx
SA56614-27GW	AAVx
SA56614-28GW	AAWx
SA56614-29GW	AAXx
SA56614-30GW	AAYx
SA56614-31GW	AAZx
SA56614-42GW	ABAx
SA56614-43GW	ABBx
SA56614-44GW	ABCx
SA56614-45GW	ABDx
SA56614-46GW	ABEx
SA56614-47GW	ABFx

PIN CONFIGURATION

SL01360
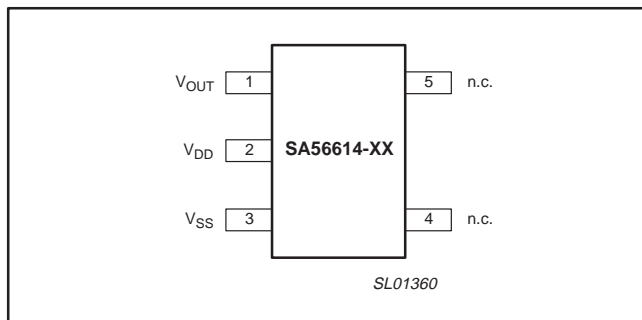
Figure 2. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	V_{OUT}	Reset HIGH output.
2	V_{DD}	Positive supply.
3	V_{SS}	Ground. Negative supply.
4	n.c.	not connected
5	n.c.	not connected

MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power supply voltage	–	12	V
V_{OUT}	Output voltage	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
I_{OUT}	Output current	–	50	mA
T_{oper}	Operating temperature	–40	85	°C
T_{stg}	Storage temperature	–40	125	°C
P	Power dissipation	–	150	mW

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DC ELECTRICAL CHARACTERISTICS

Characteristics measured with T_{amb} = 25 °C, unless otherwise specified.

| SYMBOL	PARAMETER	CONDITIONS	TEST CIRCUIT	MIN.	TYP.	MAX.	UNIT
V_S	Reset detection threshold		1 Fig. 16	$V_S - 2\%$	V_S	$V_S + 2\%$	V
ΔV_S	Hysteresis	$V_{DD} = 0\ V \rightarrow V_S + 1.0\ V \rightarrow 0\ V$		$V_S \times 0.03$	$V_S \times 0.05$	$V_S \times 0.08$	V
$V_S/\Delta T$	Threshold voltage temperature coefficient	$-40\ °C \leq T_{amb} \leq +85\ °C$		–	± 0.01	–	%/°C
I_{CC}	Supply current	$V_{DD} = V_S + 1.0\ V$		–	0.25	1.0	µA
I_{OH}	I_{DS} leakage current when OFF	$V_{DD} = V_{DS} = 10\ V$	3 Fig. 18	–	–	0.1	µA
I_{NDS1}	N-channel I_{DS} output sink current 1	$V_{DD} = 1.2\ V$; $V_{DS} = 0.5\ V$	2 Fig. 17	−0.23	0.50	–	mA
I_{NDS2}	N-channel I_{DS} output sink current 2 (for $V_S > 2.6\ V$)	$V_{DS} = 0.5\ V$; $V_{DD} = 2.4\ V$		−1.6	−3.7	–	mA
I_{NDS3}	N-channel I_{DS} output sink current 3 (for $V_S > 3.9\ V$)	$V_{DS} = 0.5\ V$; $V_{DD} = 3.6\ V$		−3.2	−7.00	–	mA
I_{PDS1}	P-channel I_{DS} output source current 1 (for $V_S < 4.0\ V$)	$V_{DS} = 0.5\ V$; $V_{DD} = 4.8\ V$	3 Fig. 18	0.36	0.62	–	mA
I_{PDS2}	P-channel I_{DS} output source current 2 (for $4.0\ V < V_S < 5.7\ V$)	$V_{DS} = 0.5\ V$; $V_{DD} = 6.0\ V$		0.46	0.75	–	mA
I_{PDS3}	P-channel I_{DS} output source current 3 (for $V_S \geq 5.7\ V$)	$V_{DS} = 0.5\ V$; $V_{DD} = 8.4\ V$		0.59	0.96	–	mA

TYPICAL PERFORMANCE CURVES
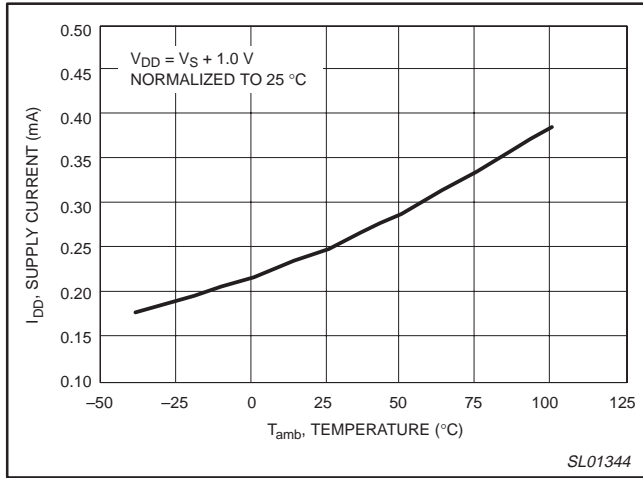
Figure 3. Supply current versus temperature.
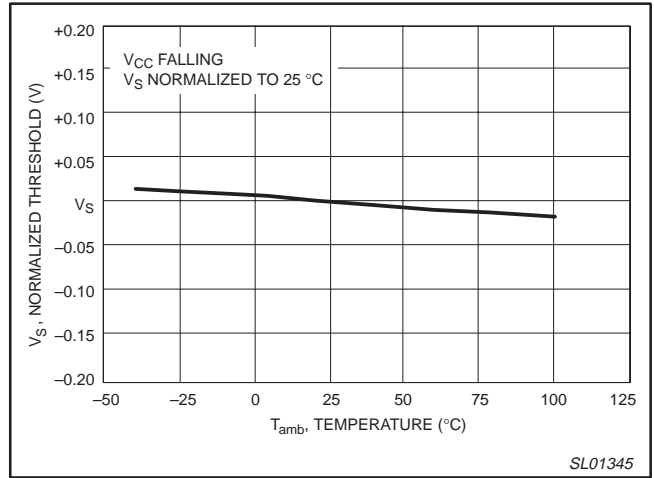

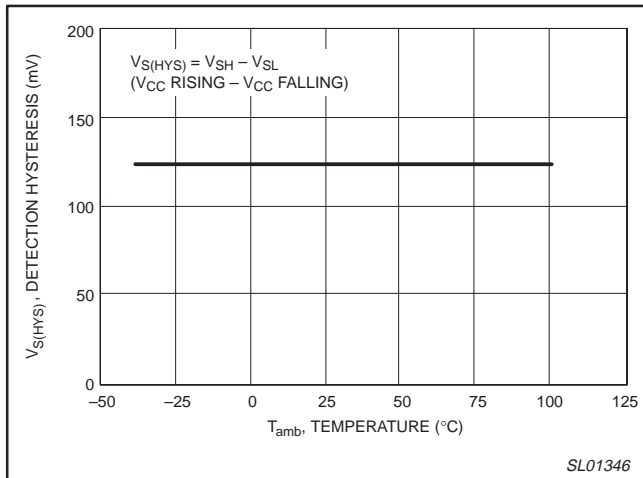Figure 4. Detection threshold versus temperature.
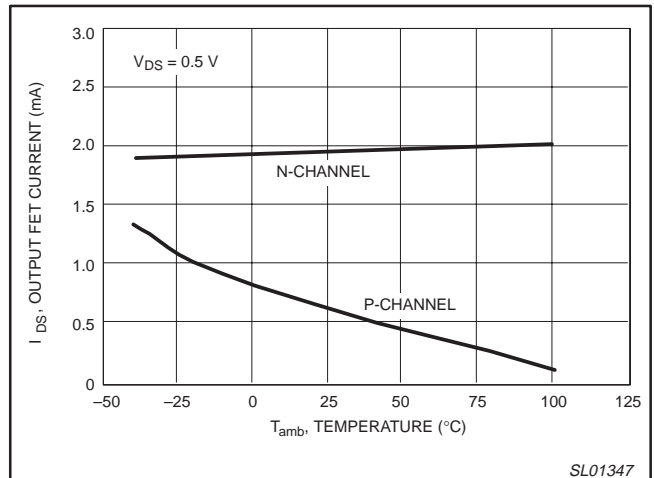

Figure 5. Detection hysteresis versus temperature.

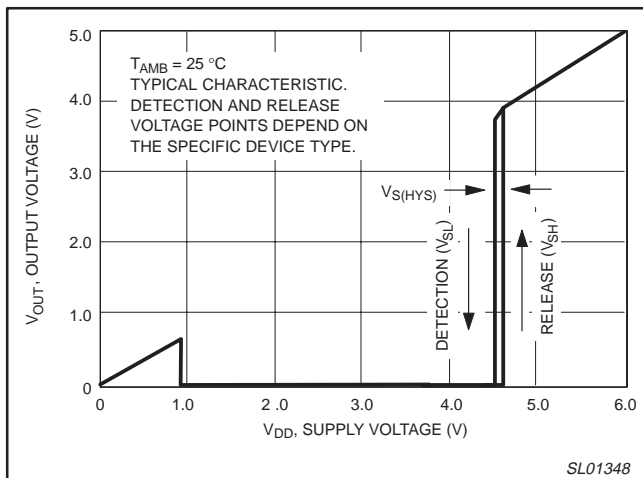Figure 6. Output FET current versus temperature.
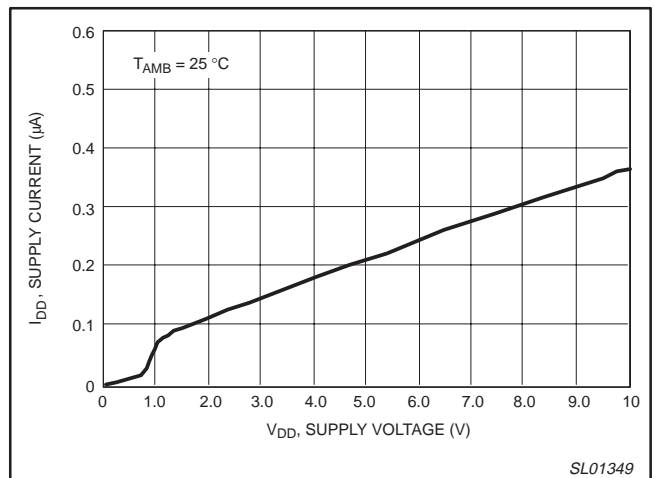

Figure 7. Output voltage versus supply voltage.
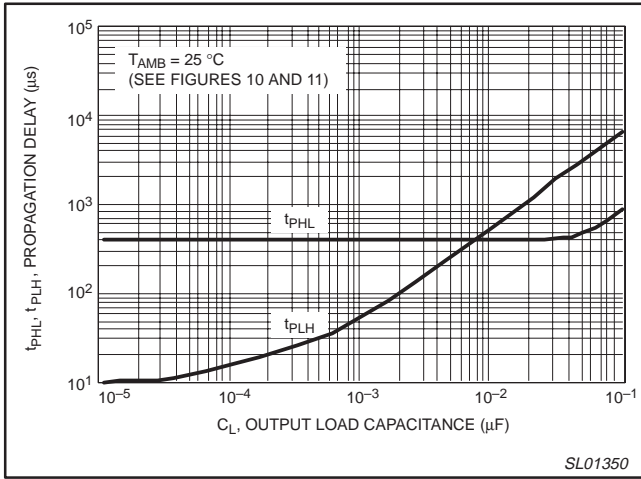

Figure 8. Supply current versus supply voltage.

Figure 9. Propagation delay versus output load C.

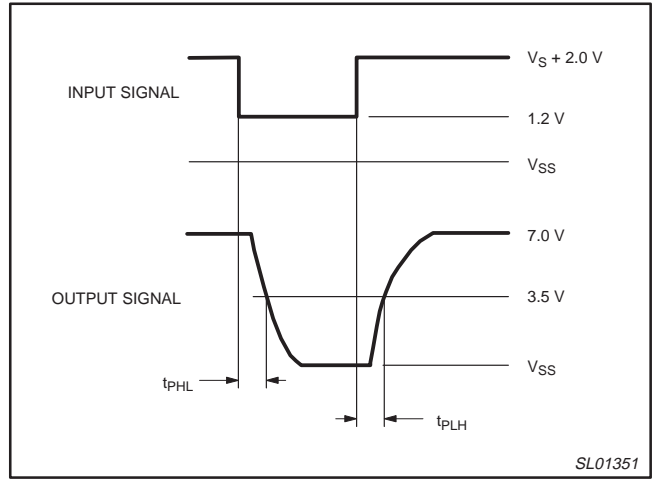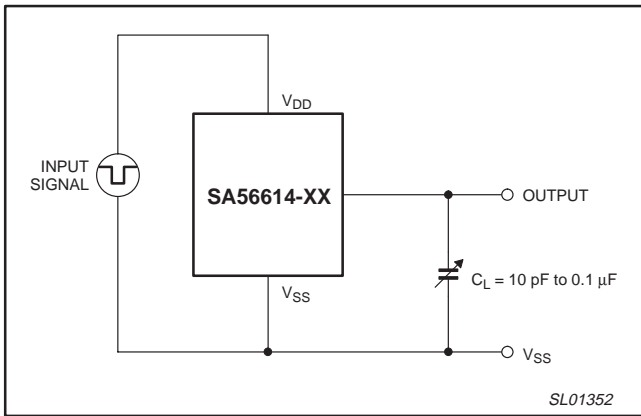

Figure 10. Propagation delay measurements.

Figure 11. Propagation delay measurement circuit.

TECHNICAL DESCRIPTION

The SA56614-XX is a CMOS device designed to monitor the system's power source and provide a system reset function in the event the supply voltage sags below an acceptable level for the system to reliably operate. The SA56614 generates a compatible reset signal for a wide variety of microprocessor and logic systems. The reset threshold incorporates a typical hysteresis of $(V_S \times 0.05)$ volts to prevent erratic resets from being generated. The SA56614 operates at very low supply currents, typically 0.25 μA, while offering a high precision of threshold detection ($\pm 2\%$).

The output of the SA56614 incorporates an active Totem-Pole output topology comprised of complimentary P-Channel and N-Channel FETs. A P-Channel FET is on the high supply side and when ON pulls the output to or near the V_{DD} supply voltage from which output source current can be obtained. A complimentary N-Channel FET is on the low or ground side, and actively pulls the output LOW or to ground with the capability of sinking current into the output. Both devices supply system reset signals. The user should keep in mind, when connecting the SA56614 to a system, the effect of supplying source current from the output of the SA56614 on the system. This is of particular importance where the SA56614 is operated from a different supply source than the rest of the system.

Figure 12 is a functional block diagram of the SA56614. The internal reference source voltage (V_{REF}) is typically 0.8 V over the operating temperature range. The reference voltage is connected to the non-inverting input of the threshold comparator while the inverting input monitors the supply voltage through a resistor divider network made up of R_1, R_2, and R_3. The output of the threshold comparator drives the totem-pole output stage of the device.

When the supply voltage sags to the threshold detection voltage, the resistor divider network supplies a voltage to the inverting input of the threshold comparator which is less than that of V_{REF}, causing the output of the comparator to adopt a HIGH output state. This causes the high side P-Channel FET of the Totem-Pole output stage to turn OFF while simultaneously turning the low side N-Channel FET from OFF to an active ON state, pulling the output to a LOW voltage state. The device adheres to a true input/output logic protocol. The output goes to a LOW voltage state when input is

LOW (below V_S) and the output HIGH goes to a HIGH voltage state when the input is HIGH (above V_S).

The low side N-Channel FET (TR_3) establishes threshold hysteresis by turning ON whenever the threshold comparator's output goes to a HIGH state (when V_{DD} sags to or below the threshold level). TR_3's turning ON causes additional current to flow through resistors R_1, and R_2 causing the inverting input of the threshold comparator to be pulled even lower. For the comparator to reverse its output polarity and turn OFF TR_3, the V_{DD} source voltage must overcome this additional pull-down voltage present on the comparator's inverting input. The differential voltage required to do this establishes the hysteresis voltage of the sensed threshold voltage. Typically it is $(V_S \times 0.05)$ volts.

When the V_{DD} voltage sags and is at or below the Detection Threshold (V_{SL}), the device will assert a Reset LOW output at or very near ground potential. As the V_{DD} voltage rises from ($V_{DD} < V_{SL}$) to V_{SH} or higher, the reset is released and the output follows V_{DD}. Conversely, decreases in V_{DD} from ($V_{DD} > V_{SL}$) to V_{SL} or lower cause the output to be pulled to ground.

Hysteresis Voltage = Release Voltage – Detection Threshold Voltage

$$V_{HYS} = V_{SH} - V_{SL}$$

where:

$$V_{SH} = V_{SL} + V_{HYS} \cong V_{REF}(R_1 + R_2) / R_2$$
$$V_{SL} = V_{REF}(R_1 + R_2 + R_3) / (R_2 + R_3)$$

When V_{DD} drops below the minimum operating voltage, typically less than 0.95 volts, the output is undefined and output reset low assertion is not guaranteed. At this level of V_{DD} the output will try to rise to V_{DD}.

The V_{REF} voltage is typically 0.8 V. The devices are fabricated using a high resistance CMOS process and utilize high resistance R_1, R_2, and R_3 values requiring very small amounts of current. This combination achieves very efficient low power performance over the full operating temperature.
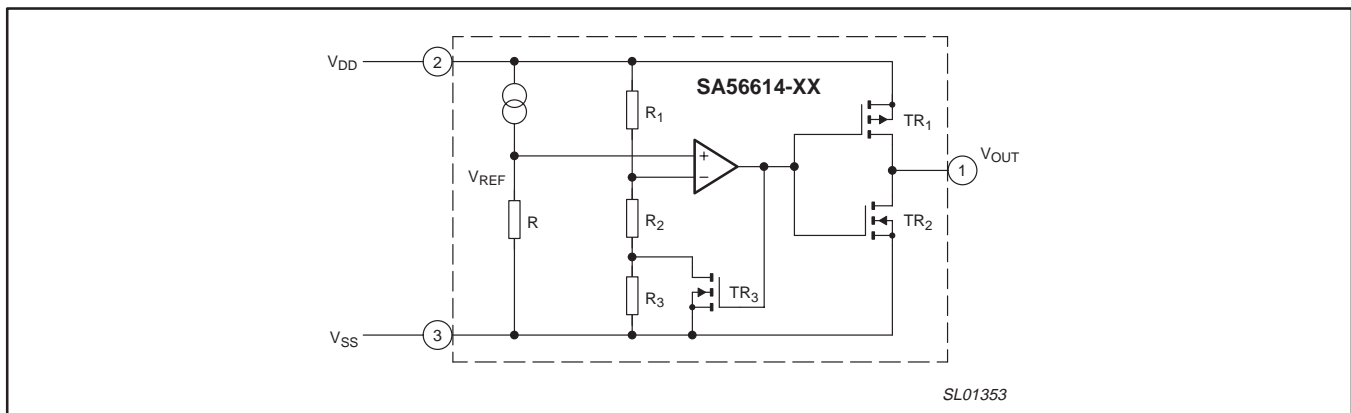

Figure 12. Functional diagram

TIMING DIAGRAM

The timing diagram shown in Figure 13 depicts the operation of the device. Letters A-J on the TIME axis indicate specific events.

A: At 'A', V_{DD} begins to increase. Also the V_{OUT} voltage initially increases but abruptly decreases when V_{DD} reaches the level (approximately 0.8 V) that activates the internal bias circuitry and $\overline{RESET}$ is asserted.

B: At 'B', V_{DD} reaches the threshold level of V_{SH}. At this point the device releases the hold on the V_{OUT} reset. The Reset output V_{OUT} tracks V_{DD} as it rises above V_{SH} (assuming the reset pull-up resistor R_{PU} is connected to V_{DD}). In a microprocessor based system these events release the reset from the microprocessor, allowing the microprocessor to function normally.

C-D: At 'C', V_{DD} begins to fall, causing V_{OUT} to follow. V_{DD} continues to fall until the V_{SL} undervoltage detection threshold is reached at 'D'. This causes a reset signal to be generated (V_{OUT} Reset goes LOW).

D-E: Between 'D' and 'E', V_{DD} starts rising.

E: At 'E', V_{DD} rises to the V_{SH}. Once again, the device releases the hold on the V_{OUT} reset. The Reset output V_{OUT} tracks V_{DD} as it rises above V_{SH}.

F-G: At 'F', V_{DD} is above the upper threshold and begins to fall, causing V_{OUT} to follow it. As long as V_{DD} remains above the V_{SH}, no reset signal will be triggered. Before V_{DD} falls to the V_{SH}, it begins to rise, causing V_{OUT} to follow it. At 'G', V_{DD} returns to normal.

H: At event 'H' V_{DD} falls until the V_{SL} undervoltage detection threshold point is reached. At this level, a $\overline{RESET}$ signal is generated and V_{OUT} goes LOW.

J: At 'J' the V_{DD} voltage has decreased until normal internal circuit bias is unable to maintain a V_{OUT} reset. As a result, V_{DD} may rise to less than 0.8 V. As V_{DD} decreases further, V_{OUT} reset also decreases to zero.
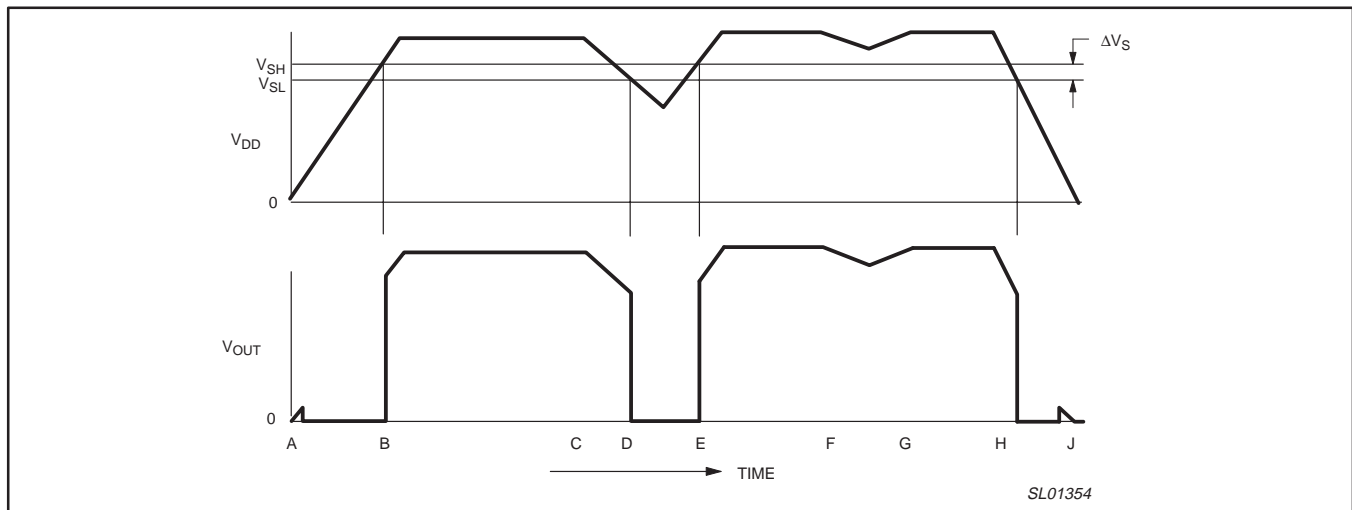

Figure 13. Timing diagram.

APPLICATION INFORMATION

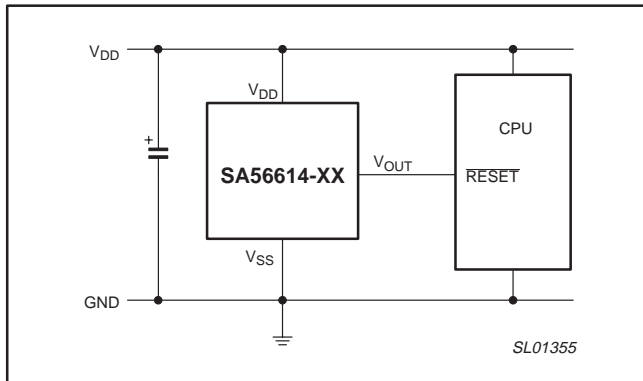**Figure 14. Conventional reset application**

Figure 15. High impedance supply operating problems

Small changes in supply current will occur when the SA56614 asserts or releases a reset. In some cases this can cause oscillations of the device. This can present a problem, particularly where high impedance V_{DD} sources are employed. Figure 15 shows how this may occur.
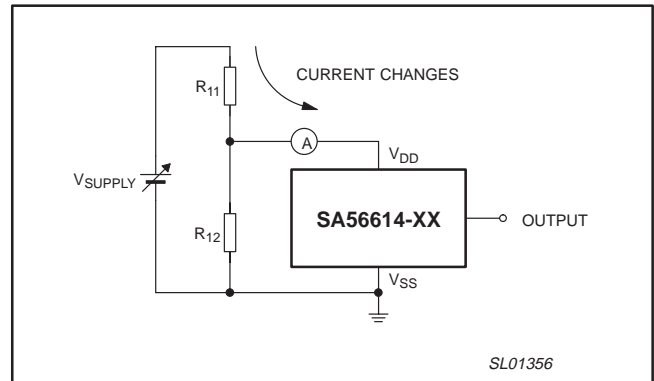
Significant voltage variations of V_{DD} may occur when the device is operated from high impedance power sources. When the device asserts or releases a reset, V_{DD} variations are produced as a result of the voltage drop developed across R_{11} due to the current variations through the resistor R_{11} (representing the supply impedance). If the V_{DD} variations are large, such that they exceed the Detection Hysteresis, the output of the device can oscillate from a HIGH state to a LOW state. The user should avoid using high impedance V_{DD} sources to prevent such situations.
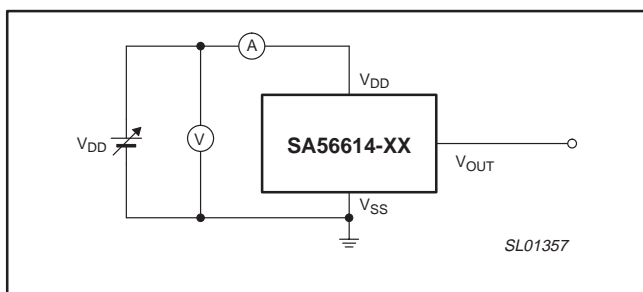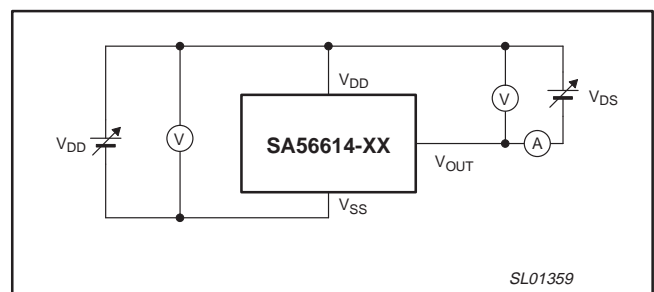
TEST CIRCUITS

Figure 16. Test Circuit 1
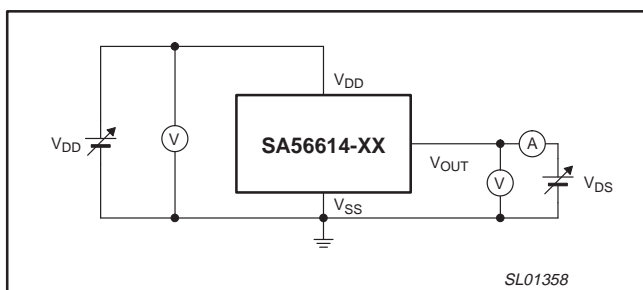

Figure 18. Test Circuit 3

Figure 17. Test Circuit 2

PACKING METHOD

GUARD BAND

TAPE

REEL ASSEMBLY

BARCODE LABEL

BOX

TAPE DETAIL

COVER TAPE

CARRIER TAPE

SL01305
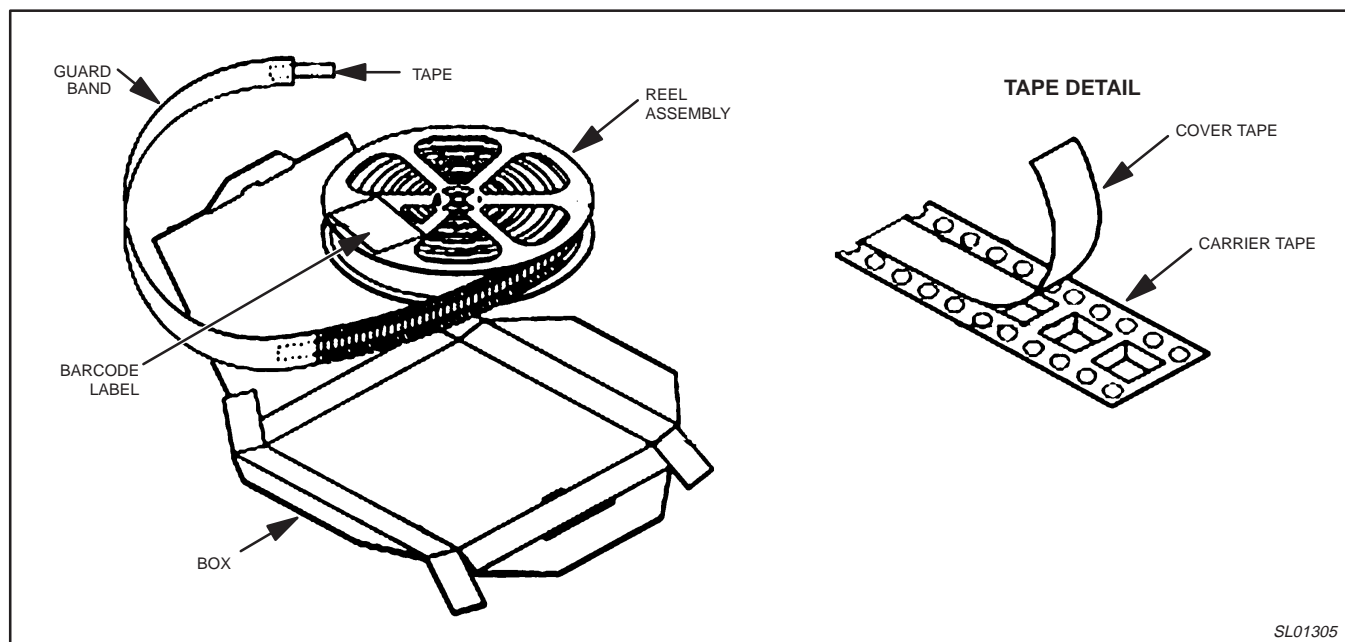
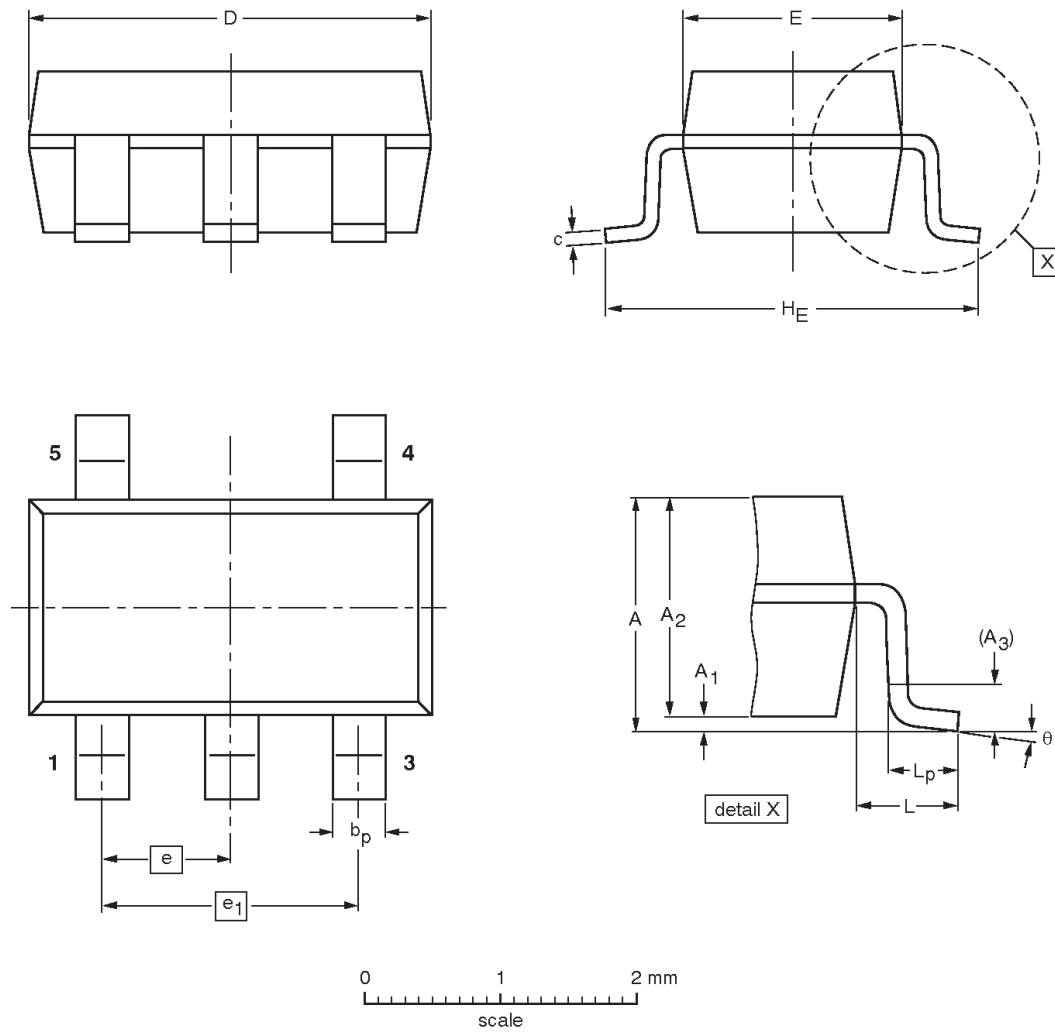**Figure 19. Tape and reel packing method**

Plastic small outline package; 5 leads; body width 1.6 mm　　　　　　　　　　　　　　　　**SOP003**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	e_1	H_E	L	L_p	θ
mm	1.35	0.15 0.05	1.2 1.0	0.25	0.50 0.25	0.22 0.08	3.0 2.7	1.7 1.5	0.95	1.9	3.0 2.6	0.6	0.55 0.35	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOP003		MO-178				~~03-06-25~~ 03-10-07

REVISION HISTORY

Rev	Date	Description
_6	20031030	**Product data (9397 750 12212). ECN 853-2248 30320 of 09 September 2003.** **Supersedes data of 2003 Jul 31 (9397 750 11847).** Modifications: ● Change package outline version to SOP003 in Ordering information table and Package outline sections.
_5	20030731	**Product data (9397 750 11847). ECN 853-2248 30164 of 30 July 2003.** **Supersedes data of 2003 May 12 (9397 750 11495).**
_4	20030512	**Product data (9397 750 11495). ECN 853-2248 29012 of 04 October 2002.** **Supersedes data of 2002 Sep 13 (9397 750 10401).**
_3	20020913	**Product data (9397 750 10401). ECN 853-2248 28914 of 13 September 2002.** **Supersedes data of 2001 Jun 19.**

CMOS system reset

SA56614-XX

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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